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THESIS

MODELING THE QUANTUM DOT

by

Suzanne L. Kruppa

June, 1997

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Quantum device performance is extremely sensitive to small variations in design parameters. Accurate theoretical modeling is therefore required to guide the technology development. Conventional device design tools are based on classical physics, and do not incorporate quantum effects. New design tools are required to explicitly account for the quantum effects that control charge transport at the nanometer scale. To further understand and develop nanoscale device technology, this thesis will model the potential energy function in a quantum dot, a nanostructure in which electrons are quantum-mechanically confined in all three dimensions and which represents the inevitable result of continued downscaling of semiconductor devices.

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MODELING THE QUANTUM DOT

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Submitted in partial fulfillment
of the requirements for the degree of

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ABSTRACT

Much of the progress in solid-state microelectronics has come from the continued reduction in size of the transistors that make up integrated circuits (ICs), having dropped by a factor of 10 in the last decade to where minimum device geometries have reached approximately 350 nanometers in mass production. Continued improvements in ICs will require a device technology that can be scaled down to the sub-100 nanometer size regime. There, the quantum mechanical nature of the electron becomes strongly evident, and new design tools are required for a *nano*-electronic semiconductor technology. The combined scaling and speed advantages of these new devices could portend orders of magnitude increases in the functional performance of future-generation ICs.

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The author also wants to thank Professor Luscombe for his guidance and patience during the work in performing this investigation.

I. INTRODUCTION

The electronic devices that make up present-production integrated circuits (ICs) have characteristic length scales of approximately 350 nanometers. From extrapolations of the historic trend in device miniaturization, it is expected that sub-100 nanometer-scale devices will be required in the next few years for future generations of ICs. An essential characteristic of these nanoelectronic devices is that the electron wavelength becomes comparable to the device size (the room temperature de Broglie wavelength in Gallium Arsenide (GaAs), for example, is about 30 nanometers). In this regime, the fundamental quantum properties of the electron, in particular, its wave nature, dominate charge transport. It is well established that electrons have wave-like properties because interference effects such as diffraction have been observed. These interference effects must be caused by some quantity whose behavior is oscillatory and which obeys the superposition principle. This quantity is complex-valued and is referred to as the wavefunction. [Ref. 1].

Consider the effect of the wave nature of matter on quantum confinement. When an electron is confined to a region with dimensions comparable to its wavelength, its allowed energies become quantized or restricted to certain discrete levels, analogous to the allowed modes of a waveguide. In the case of a superlattice, as is found in some of the resonant tunneling transistor designs, the allowed energies further group themselves into bands which are separated by gaps of forbidden energies. The existence of these gaps is due to the interplay between the electron wavelength and the spatial periodicity of the

potential energy. In summary, the quantum confinement effect occurs in the nanometer regime, and is a basic quantum transport phenomenon which can be exploited for electronic device applications. [Ref. 2]

While the simplest practical nanoelectronic device is the resonant tunneling diode (RTD), its mode of operation is typical of that of more complex quantum devices. In the resonant tunneling diode, a one dimensional quantum well structure, in which an electron is quantum-mechanically confined in one direction (but is otherwise free in the remaining two dimensions) is used to produce a nonlinear device characteristic that has innovative circuit applications. Such a structure is said to exhibit one dimensional quantum confinement. While to date the most progress has been achieved with one dimensional quantum devices, e.g., resonant-tunneling transistors and integrated circuits, devices have also been fabricated which feature two and three dimensional quantum confinement, and are termed quantum wire and quantum dot structures, respectively. Quantum dots, as shown in the scanning electron micrograph of Figure 1, are the inevitable result of continued downscaling of semiconductor structures and probably represent the smallest possible noncryogenic switching devices. Thus, the development of one, two, and three dimensional quantum dots provides a progression toward the ultimate scaling limits of solid state electronics.

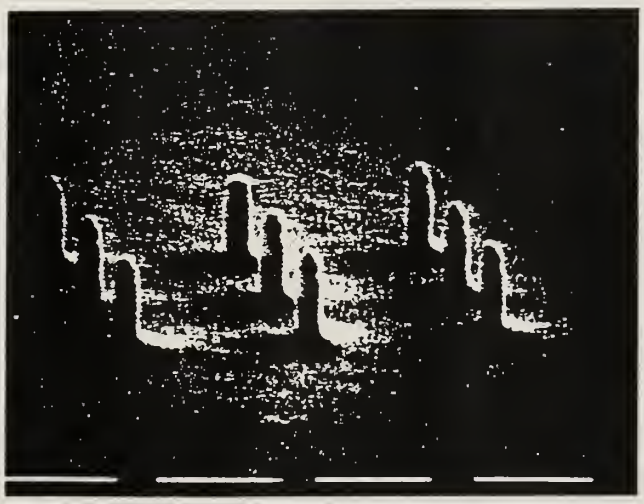

Figure 1 - Array of etched quantum dots. The horizontal markers are 500 nm in length; the diameter of each dot is 100 nm. From Ref. [2].

II. DEVICE MODELING

A. STATUS OF CURRENT MODELING TECHNIQUES

Current IC technology is based on devices with minimum feature sizes of approximately 350 nanometers. The characteristics of such devices can be quantitatively described with models based on semiclassical physics and whose transport features can be described by means of Maxwell-Boltzmann statistical distributions. The current approach assumes that scattering is a process unrelated to the device electrical fields and that it occurs instantaneously, both temporally and spatially. This approach further assumes that electron potential and density gradients are weak in the sub-100 nanometer regime. Under these assumptions, present-generation devices are extensively modeled using commercially available software design tools before fabrication is ever attempted because the complexity of microelectronic devices is such that computer simulation is the only practical means of producing realistic designs. An experimental approach based solely on "trial-and-error" would prove prohibitively expensive and time-consuming. Since conventional device design tools are based on classical current-flow models, they do not incorporate quantum effects and are of use only when the underlying quantum mechanical effects can be hidden behind an average macroscopic parameter such as the electron mobility. Obviously, charge transport in future device designs must be described in a way that accounts for quantum effects. [Ref. 4]

B. NEED FOR NANOELECTRONIC MODELING TECHNIQUES

New design tools are required to explicitly account for the quantum effects that control charge transport at the nanometer scale. Moreover, the need for modeling is even greater at the nanoscale than it is in the submicrometer regime because the electrical performance of quantum devices can be acutely sensitive to small variations in design parameters. Quantum devices make use of the energy levels of confined electrons to control the flow of charge, and the potential energy environment that gives rise to such levels is a strong function of the geometry and layer properties of the device structure. The number of critical design variables also increases with the number of quantum confinement dimensions. Thus, the development of future nanoscale devices that exploit multidimensional quantum confinement effects will require even more sophisticated quantum modeling tools. This thesis will take a first step in this direction by modeling the self-consistent electron potential of a nanoelectronic quantum dot in the absence of applied voltage. [Ref. 2]

III. HETEROJUNCTIONS AND HETEROSTRUCTURES

A. HETEROJUNCTIONS

Figure 2 illustrates the atomic arrangement in a crystal in which a compound semiconductor (like GaAs) has been grown upon an elemental semiconductor like Germanium (Ge), resulting in an abrupt change in chemical composition at the boundary.

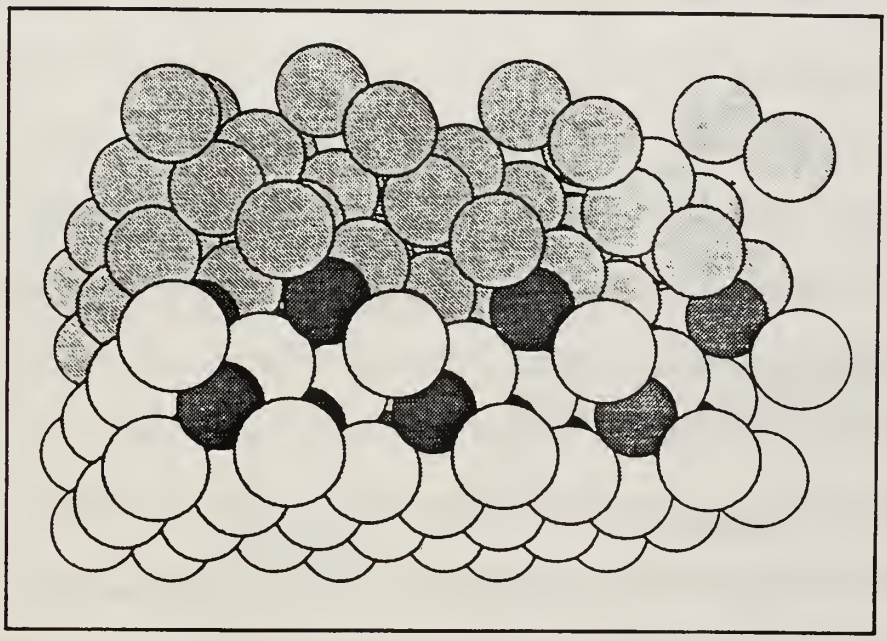

Figure 2 - Atomic structure of a heterostructure. From Ref. [5]

The lighter gray spheres are the Gallium atoms, the medium gray shows the Germanium atoms, and the darker gray shows the Arsenic atoms. While a continuous network of covalent bonds is observed throughout the structure, it is apparent the types of atoms bond in a layered structure, called a heterojunction. The construction of additional layers results in formation of a heterostructure. The energy-band profile of a typical heterojunction is shown in Figure 3. The

band structure depends upon the chemical composition which explains the unique band gap across each heterojunction.

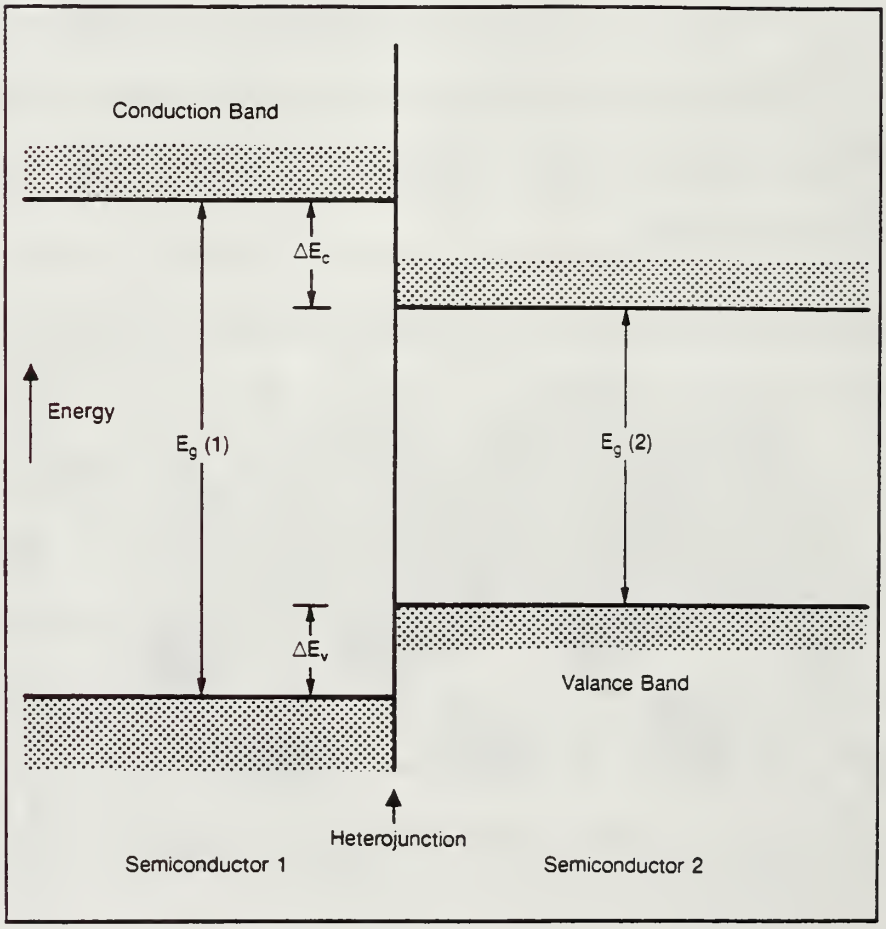

Figure 3 - Band profile of a typical heterojunction. From Ref. [5].

B. QUANTUM HETEROSTRUCTURES

The advantage of using heterostructures in quantum device design and fabrication is that we may use wavefunction engineering to exploit the wave nature of the electron. Wavefunction engineering is defined as the manipulation of heterostructures and corresponding bandgaps for device design. It is based

on the principle that the wavefunction obeys the Schrödinger equation. The frequency with which the wavefunction oscillates is proportional to the total energy of the electron, and its wave vector is proportional to the momentum. Likewise, the probability density of finding an electron at a particular place is proportional to the squared magnitude of the wavefunction. [Ref. 1] Extremely useful quantum effects occur when the potential energy of the electron (as a function of position) has some abrupt features, as can be accomplished using heterojunctions. The effective potential for conduction electrons (with no kinetic energy) in a semiconductor is defined as the energy of the bottom of the conduction band. Specific examples of the bandgaps of various combinations of materials are illustrated in Figure 4. As can be seen, particularly in (a), (b) and (c) of that figure, a layer of wider-bandgap semiconductor acts like an energy barrier for electrons in the conduction band of a narrower-bandgap semiconductor. These energy barriers can be used to confine electrons to small regions of a device. Such a small region of narrower-gap semiconductor bounded on two sides by regions of wider-gap semiconductor is called a quantum well. In a quantum well, the electron is repeatedly reflected between the energy barriers which sets up a standing wave pattern at a discrete frequency. Discrete frequencies correspond to discrete energies, as required by quantum theory, and the electrons occupying these states will occupy those energy states.

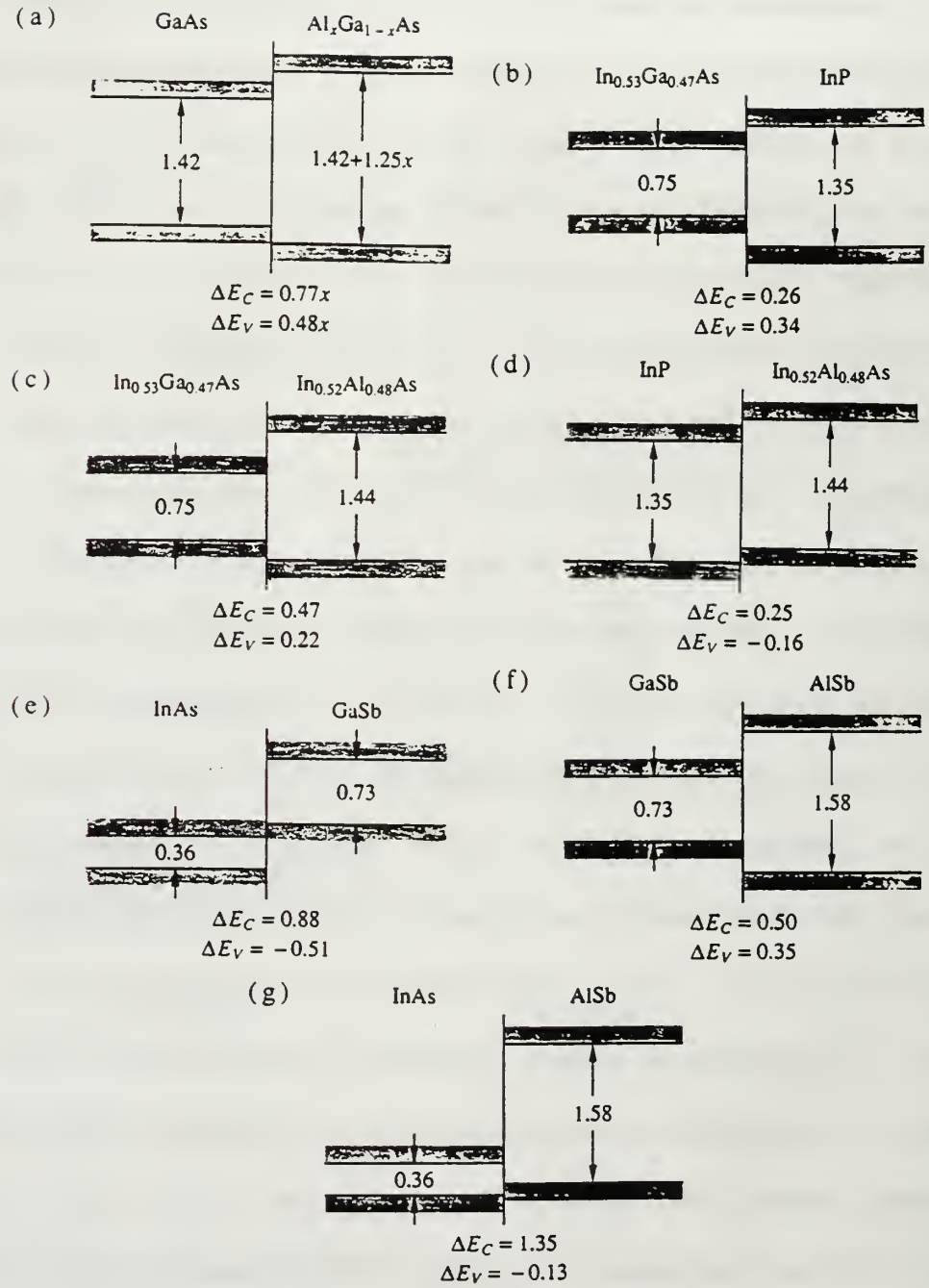

Figure 4 - Examples of bandgaps for heterojunctions of varying materials. From Refs. [6,7].

In the case of a heterostructure quantum well, the electron energy levels are determined by size quantization, because the very small size of the quantum well (a few nanometers) causes the energies of the states to be sufficiently

separated as to be easily observable. When wavefunction engineering is used to determine the size and shape of a quantum well, a heterostructure that has a particular set of energy levels can be designed. [Ref. 5]

C. QUANTUM DOT FABRICATION

Recent advances in microfabrication technology and the use of semiconductor materials where the electron effective mass is relatively small have enabled the production of quantum dot structures. Most frequently, the process begins with molecular beam epitaxy (MBE) onto a stable substrate. An MBE system is simply an ultrahigh-vacuum evaporator. By tightly controlling the temperature of the single-crystal substrate and flow rate of the evaporated molecules, high purity epitaxial growth may be achieved. Figure 5 shows an example of an MBE system. As the crystal is grown, the effusion cell shutters are opened and closed as necessary to produce the desired layering of materials. [Ref. 8] The result is either a heterojunction (the basis for an RTD) or a multi-layered heterostructure. The final step is to "core out" a section of the planar layered structure using electron-beam lithography techniques to produce a cylindrical device with a lateral dimension comparable to the quantum wavelength. Finally, a quantum dot is produced which is, essentially, a "man-made atom" in which an electron is temporarily confined in all three spatial dimensions. This three-dimensional confinement is provided by tunnel barriers in the "vertical" epitaxial growth direction and by a depletion potential (extending inwards from the lateral surfaces) in the lateral directions. Allowed energy states are thereby virtually discrete. Since the electrons can tunnel out of the quantum

dot region in finite time, they have a range of energies consistent with the uncertainty principle. These types of states are called "quasi-bound." [Ref. 9]

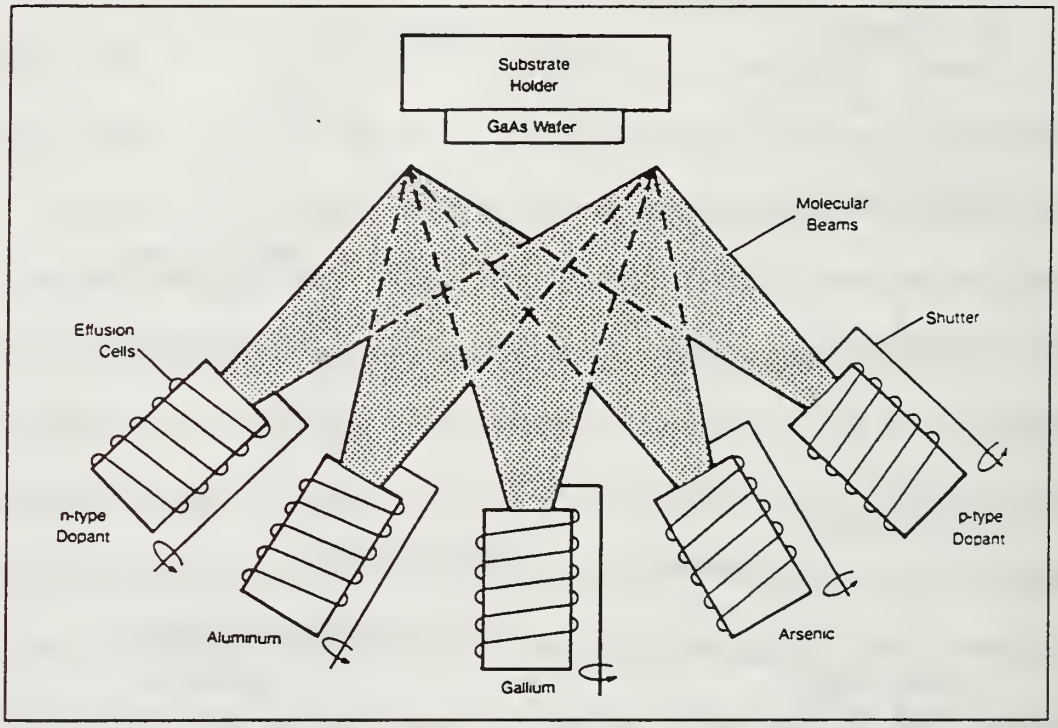

Figure 5 - Schematic of a molecular beam epitaxy system (MBE). From Ref. [5].

D. APPLICATIONS: THE RESONANT TUNNELING DIODE

The RTD is one particular device that is currently fabricated using the aforementioned MBE technique. Operation of an RTD device is similar to that of a quantum dot so a discussion of Figure 6, a typical RTD, is in order. Note the dimensions in the figure are 400-500 nanometers - much larger than those of a quantum dot. Observe in the figure that a GaAs quantum well is bounded by thin layers of AlGaAs, a semiconductor material with a larger bandgap. These layers

must be thin enough to allow current to flow through the device in a controllable fashion.

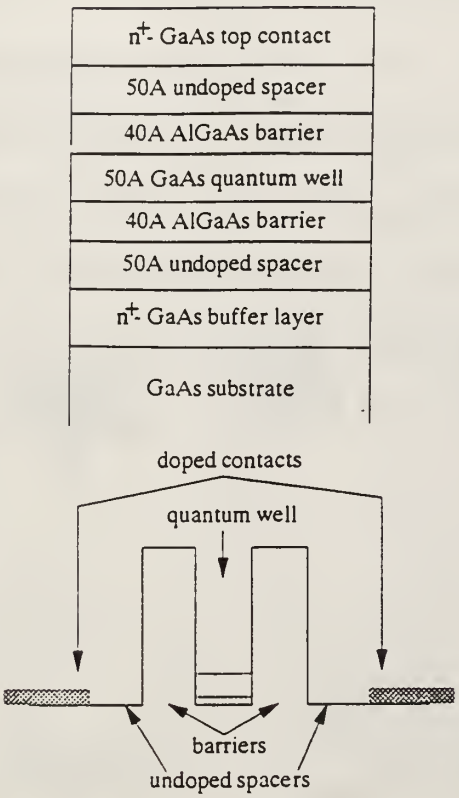

Figure 6 - Design of a typical resonant tunneling diode (RTD). From Ref. [8].

Such a flow occurs through tunneling, the quantum mechanical principle by which an electron is able to transit through a region which is classically forbidden. In this example, the contacts are doped with electrons (n-type) to facilitate tunneling upon application of a bias to the device. The function of the two undoped spacer layers is to reduce the diffusion of charge carriers into the quantum well/barrier system and thereby reduce electron scattering which would

further broaden the electron states in the quantum well. In order to tunnel, an electron must have exactly the same energy as that of the discrete state in the quantum well. [Ref. 8] This may be accomplished by applying a voltage to one side, as shown in Figure 7.

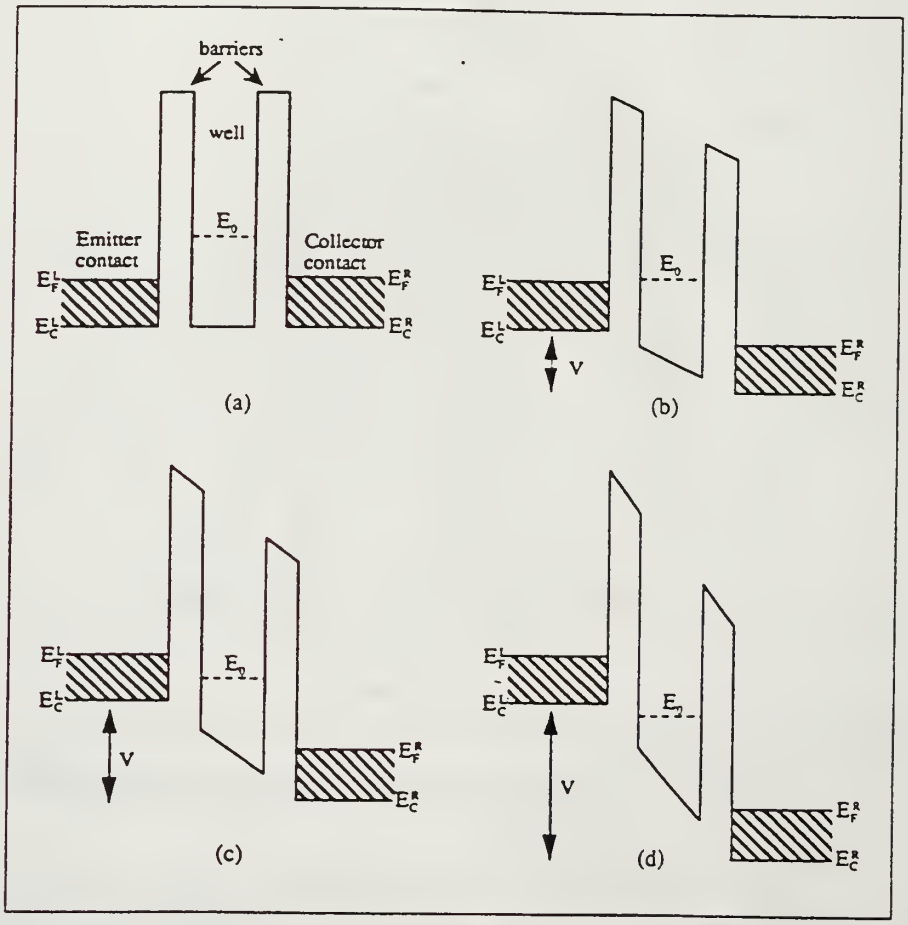

Figure 7 - Resonant tunneling diode without (a) and with (b,c,d) applied bias From Ref. [10].

In the figure, E_F^L and E_F^R represent the Fermi level in the emitter and collector, respectively. E_0 is the energy level at which tunneling occurs, and E_C^L and E_C^R represent the energies of the conduction band edge of the emitter and collector, respectively. In 7 (a), there is no applied voltage so tunneling does not occur. A

low voltage is applied in 7 (b), still insufficient for significant current flow, though some electrons will move through. When the voltage is increased, as shown in 7 (c), a resonance is reached whereby the electron energy on the emitter side equals the energy state of the well. At that point, electrons are able to tunnel through the barrier and current flows at a maximum level. This situation is defined as a resonance. If one continues to increase the applied voltage, the energy levels of the electrons will no longer match the level in the well, as can be observed in 7 (d), and current flow will slow dramatically and eventually stop. [Ref. 11] This situation can be described graphically by Figure 8, a typical IV curve (current versus voltage) for an RTD.

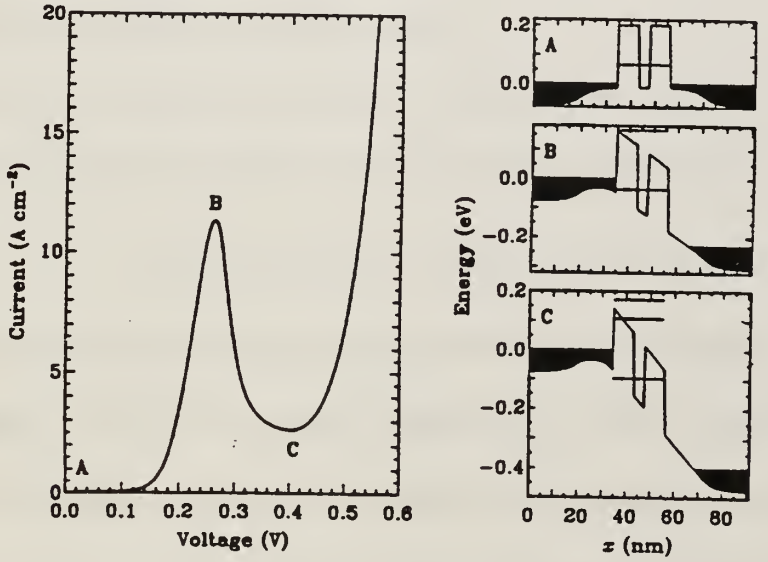

Figure 8 - Typical current versus voltage (IV) curve for an RTD showing the energy levels corresponding to the inflection points. From Ref. [12].

IV. TECHNICAL APPROACH

A. OVERVIEW

One of the foremost quantities of interest in designing and understanding quantum devices is the potential energy environment inside the device. Most, if not all, of the insight necessary to understand device operation can be obtained once this information is known. In addition, if the potential energy of the carriers as a function of position within the device has been reliably determined, one can then realistically calculate the internal laterally quantized energy levels that govern the transport characteristics of quantum dots. Therefore, the primary focus of this thesis is directed toward modeling and describing the potential energy environment within quantum dots.

B. POISSON SCHRÖDINGER APPROACH

A conventional starting point for modeling the electron states of semiconductors is to solve the effective-mass Schrödinger equation,

$$\frac{-\hbar^2}{2}\nabla\cdot\left(\frac{1}{m^*(\vec{r})}\nabla\right)\psi(\vec{r}) + V(\vec{r})\psi(\vec{r}) = E\psi(\vec{r}), \qquad (1)$$

subject to the boundary conditions imposed by the device geometry. Here $\hbar$ is Planck's constant, $m^*(\vec{r})$ is the electron effective mass, which varies from layer to layer of heterostructure systems, $V(\vec{r})$ is the electron potential energy function within the device, $\psi(\vec{r})$ is the electron wave function and E is the total electron energy. In the effective mass approach, one replaces the effects of the band structure of the material with a single parameter, the effective mass, m^*. One

therefore treats the electron in a semiconductor as if it were a free particle having effective mass m^*.

Obviously, a crucial piece of information that enters the Schrödinger equation is the potential energy function, $V(\vec{r})$. [Ref. 1] This is the part of the potential energy that is related to changes in the device. This quantity must be obtained from a calculation, by solving the Poisson equation, which relates $V(\vec{r})$ to the net charge density function within the device, $\rho(\vec{r})$,

$$\nabla \cdot \left(\varepsilon(\vec{r})\nabla V(\vec{r})\right) = e\rho(\vec{r}) = e^2\left\{N_d(\vec{r}) - n\left[V(\vec{r})\right]\right\}. \qquad (2)$$

Here $\varepsilon(\vec{r})$ is the dielectric constant, which varies from layer to layer of heterostructure systems, $N_d(\vec{r})$ is the spatially varying doping density, e is the magnitude of the electronic charge, and n is the number density function for conduction electrons. A complicating factor in the semiconductor modeling problem is that the conduction electrons are free to move around in the device, and hence to alter their spatial density, in response to the electrostatic potential. Thus, the device electron density function is actually a functional of the electron potential energy function, and is described by the relationship $n(\vec{r}) = n\left[V(\vec{r})\right]$. Equation (2) is therefore a nonlinear Poisson equation where the potential energy and the electron density functions must be determined simultaneously, or *self*-consistently, subject to the boundary conditions imposed by the device structure. [Ref. 13]

C. FINITE TEMPERATURE THOMAS-FERMI THEORY

An alternative to the Schrödinger Poisson approach is to assume that the electron states are plane waves and use an approximation technique to

determine the charge density function, which precludes having to solve the Schrödinger equation for the actual electron wavefunction. This approach is known as the Thomas-Fermi (TF) theory of the electron density, generalized to the requirement of finite device temperature. In this approach, the electron density function, $n(\vec{r},T)$, at a temperature T, is taken to be given by

$$n(\vec{r},T) = N_C(\vec{r},T)F_{\frac{1}{2}}\left[\left(E_F - E_C(\vec{r})\right)/k_BT\right] \qquad (3)$$

where $N_C(\vec{r},T) \equiv 2\left[m^*(\vec{r})k_BT/\left(2\pi\hbar^2\right)\right]^{3/2}$, with $m^*(\vec{r})$ the effective mass for each heterolayer, k_B Boltzmann's constant, E_F the Fermi level energy, and the function $F_{1/2}$ is a Fermi-Dirac integral, conventionally defined by

$$F_{\frac{1}{2}}(\eta) = \frac{2}{\sqrt{\pi}}\int_0^\infty dx\, x^{1/2}[1+\exp(x-\eta)]^{-1}. \qquad (4)$$

To derive Equation (3), one assumes that the local density function is equal to, at any point in the device, the density found in a bulk system with uniform potential and equivalent Fermi levels. In quantum devices, this assumption is only approximately correct. [Ref. 14] J.H. Luscombe and coworkers at the Texas Instruments Central Research Laboratory researched the applicability of the TF approach and related the effective mass assumption to device modeling. They determined that results obtained within the Thomas-Fermi approach are consistent with the more accurate and realistic Poisson Schrödinger method. [Ref. 2] Consequently, the TF approach is the one used to model electron potential energies in this thesis. Equation (3) must be solved iteratively to achieve a self-consistent solution, since the Fermi-Dirac integral is a nonlinear

As with the Poisson Schrödinger theory, the electrons both generate an electrostatic potential, but, being mobile, are also able to respond to the potential generated by all the other charges in the system. Thus, to achieve an electron distribution in which all electrostatic forces are balanced (taking into account the quantum statistics), the Poisson equation, Equation (2), must be solved repetitively until this condition is achieved, subject to the appropriate boundary conditions. The TF theory was originally designed to model the electron density function in many-electron atoms; the same strategy can be used to model the electrons in quantum devices. This treatment of the conduction electrons is a useful theoretical approach on which to base nanostructure design tools, providing a framework for understanding the roles that such system parameters as the lateral dimensions, boundary conditions, and epitaxial structure (doping densities, band offsets, effective masses and dielectric constants) play in forming the device potential. [Ref. 15]

1. Self-Consistent Electron Potential

In quantum-effect, heterostructure-based devices, the conduction band minimum varies spatially throughout the device and is denoted by $E_c(\vec{r})$. There are two dominant contributions to this function,

$$E_c(\vec{r}) = \Delta E_c(\vec{r}) + V(\vec{r}), \qquad (5)$$

where $\Delta E_c(\vec{r})$, the conduction band offset function, denotes the conduction band minimum in a given heterolayer relative to that of some reference material in the device, and is constant within each heterolayer. The quantity $V(\vec{r})$ is the electron electrostatic potential energy discussed above, $V(\vec{r}) = -e\phi(\vec{r})$, with $\phi(\vec{r})$

device, and is constant within each heterolayer. The quantity $V(\vec{r})$ is the electron electrostatic potential energy discussed above, $V(\vec{r}) = -e\phi(\vec{r})$, with $\phi(\vec{r})$ the electrostatic potential. [Ref. 15] The Poisson equation in terms of $V(\vec{r})$ is given in Equation (2).

Historically, model development of the potential energy environment in heterostructure devices retains only the first term in Equation (5), $\Delta E_C(\vec{r})$, and is identified as the "flat-band" model. In the case of a bulk semiconductor, this can provide a reasonable first estimate of the device potential, while for quantum dot applications, this is an invalid approximation. [Ref. 15] The limitation of the flat-band model is that it ignores the numerous sources of band bending in nanostructures from, for example, Fermi level pinning, which becomes more pronounced in significance as the device structure shrinks. Therefore, to have an accurate understanding of the device potential, it is essential to solve for the potential function using Equation (2) instead of assuming it *a priori*.

Electron densities can vary by many orders of magnitude over the dimensions of the structure, from highly degenerate in certain regions, to conditions of total depletion in others. Indeed, the unique transport properties of quantum devices hinge upon the creation of this inhomogeneous electron gas, where typically a depleted tunneling region separates neighboring electron populations in equilibrium with the Fermi levels established by the respective contacts. The role of the electron potential is thus two-fold: $E_C(\vec{r})$ determines the electron states, while at the same time it is determined by the electrostatic action of the carriers in screening the dopant charges (and by the boundary

conditions imposed by the nanostructure). Reliable predictions of electron energy levels must therefore be based on self-consistent potentials. [Ref. 15]

2. Electrostatic Screening Process

The formation of the lateral confining potential, V(r), in quantum nanostructures is the result of a nonlinear, electrostatic screening process which is driven primarily by depletion properties of the system, the doping level, and the lateral dimensions. The fabrication process includes a means by which the quantum dot is cored out from a heterostructure. When this is completed, the Fermi level on the exposed, lateral surface becomes pinned to a characteristic value in the bandgap, as shown in Figure 9, a cross-sectional view of the potential energy of a quantum dot as a function of radius. Electrons are attracted to the lateral surfaces and a transfer of charge from the interior to these surfaces takes place, resulting in a depletion layer just inside the surface, the extent of which is defined as W. R is the physical radius of the column, and the vertical dashed lines show the region in which conduction occurs. E_F is the Fermi level. While this behavior is well-documented and acceptable for macroscale semiconductors devices, the depletion layer of a nanoscale device can be a significant portion of its overall size. Moreover, at some point, a quantum dot will be unable to be made smaller or total depletion will result - the ultimate limit to downscaling of quantum devices. For these reasons, Fermi level pinning and the associated depletion layer must be factored into the modeling effort. [Ref. 5]

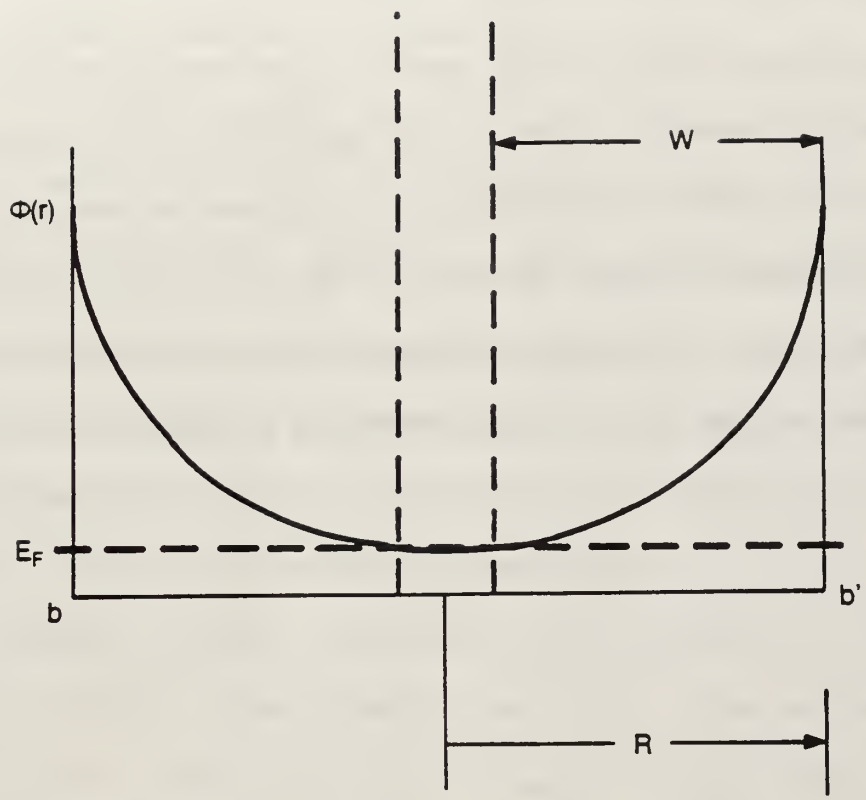

Figure 9 - Schematic illustration of the lateral (b-b') potential of a column containing a quantum dot. From Ref. [5].

To implement a self-consistent calculation requires an expression for the electron density function as a function of $E_c(\vec{r})$. As devices are made progressively smaller, it becomes necessary to increase doping concentrations to ensure an adequate supply of electrons. In the doping process, charge carriers are placed in the contacts. These electrons tunnel into the quantum well upon application of a voltage, thereby resulting in current flow through the device. Moreover, one of the rationales for quantum devices is to scale device

size down to atomic dimensions, requiring the minimization of the depletion layers. Heavy doping also works toward achieving this goal. Thus the contacts of quantum devices are heavily doped, usually to the extent that the Fermi level is pushed out of the band gap and into the conduction band. In this degenerate regime the energy distribution of a population of electrons is described, not by the classical Maxwell-Boltzmann statistics, but by the quantum Fermi-Dirac statistics. Moreover, the Fermi-Dirac distribution function takes into account the Pauli exclusion principle, another fundamental tenet of quantum theory. [Refs. 1,5]

V. MODEL DESCRIPTION

A. ASSUMPTIONS AND BOUNDARY CONDITIONS

The computer program utilized in this thesis to calculate potentials, QDOT, operates under the finite temperature Thomas-Fermi theory, as discussed in Section IV.C.. The Thomas-Fermi expression for carrier density is then combined with the Poisson equation which yields a nonlinear differential equation to solve for the self-consistent potential energy function. QDOT solves this nonlinear Poisson equation, subject to boundary conditions, using a variation of Newton's method known as nonlinear overrelaxation.

Cylindrical symmetry is assumed for the quantum dots. This allows QDOT to model only a two-dimensional, radial slice of the complete structure. Obviously, a non-cylindrical quantum dot of, say, a cube-type design, may not be properly described by QDOT. However, this is not a major limitation as most currently fabricated device structures are of the cylindrical design. An additional assumption concerns the distribution of impurities. QDOT assumes that, within each epitaxial layer, dopants can be described by their average density as they provide a uniform background of charge density. The validity of this assumption decreases with device size as inhomogeneities in the dopant distribution become more significant. In the extreme case, device operation could be influenced by the presence or absence of a single doping atom.

When solving the aforementioned nonlinear differential equation, one requires a boundary condition in the lateral dimension. This is accomplished through the phenomenon known as Fermi level pinning, discussed previously.

The result of the surface pinning is a depletion region just inside the surface which serves as the boundary.

B. MODEL INPUTS AND OUTPUTS

To run the QDOT program, the user specifies first the epitaxial structure in terms of thickness, composition, and doping density for each epitaxial layer; then the lateral information such as the radius of the post and the value of the Fermi-level pinning energy for the exposed sidewalls; and finally the temperature. The program then generates a three-dimensional figure of the self-consistent band-edge surface. The output for a typical quantum dot design is shown in Figure 10. In this design, the following data was input:

LAYER	THICKNESS(nm)	DOPING LEVEL(cm^{-3})	ALUMINUM MOLE FRACTION
CONTACT	50	2.0e18	0.0
SPACER	15	1.0e15	0.0
BARRIER	5	1.0e15	0.3
QUANTUM WELL	5	1.0e15	0.0
BARRIER	5	1.0e15	0.3
SPACER	15	1.0e15	0.0
CONTACT	50	2.0e18	0.0

RADIUS: 50NM
FERMI LEVEL PINNING VALUE: 0.7Ev
TEMPERATURE: 300K

Table 1. Model Input for a Typical Quantum Dot Device Structure

Note that device shown has no applied bias and will not conduct. However, it is easy to see by referring to Figure 7 that application of a voltage will easily enable current to flow through this modeled device. Many factors influence the size and shape of Figure 10. The predominant force in determining

the extent of the band-bending potential barrier is the degree of surface depletion. This, in turn, is controlled by the lateral dimension and the value of the Fermi level pinning energy at the sidewall. The height of the quantum well is partially controlled by the width of the spacer layers. All the above variables were investigated, with the results shown in subsequent figures. First, however, a discussion of Figure 10 is in order.

Figure 10 shows a typical (and, notwithstanding a major technological breakthrough, possibly the optimal) quantum dot design. One of the most significant attributes of these devices is the turn-on voltage. As the number of devices on a chip continues to increase, power dissipation becomes more and more of a serious concern. Power dissipation can be improved by designing devices with a lower power supply voltage requirement which will result in less energy required for switching. In Figure 10, the "pedestal," as it is referred to in this thesis, is high enough to where the device will have a fairly low turn-on voltage (about 0.7 eV), but not so low that it is unable to effectively function in a digital logic environment. There are plenty of conduction electrons (those below the Fermi level, indicated in white in (a)) and an adequate radius within which current will flow. This conduction radius is best seen in (c), the distance (about 28 nm) at which the potential line (red) crosses the Fermi level ($V(r,z) = 0$). The dimensions, both depth and width, of the barriers and quantum well are unchanged throughout all the plots as they are material dependent. All plots are based on the same materials, GaAs in the well and AlGaAs in the barriers.

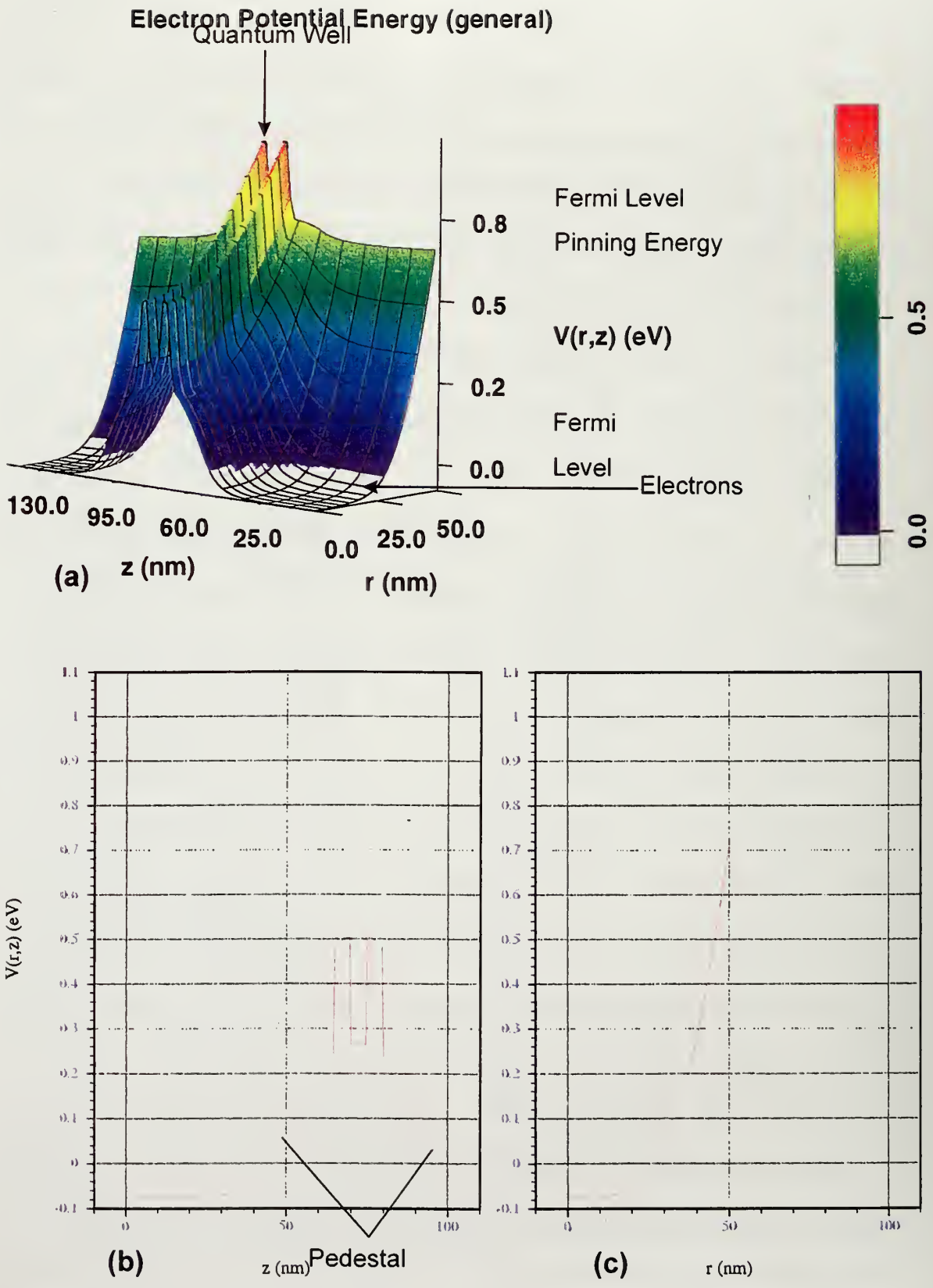

Figure 10 - Plot of a typical quantum dot with radius 50nm, Fermi level pinning of 0.7eV, and spacer width of 15nm.

VI. RESULTS

The following figures show how electron potential energy is affected by varying the radius, Fermi level pinning value, and spacer width. All plots should be compared with Figure 10 to fully understand these results.

Figure 11 shows that there is a very definite theoretical limit to quantum dot downsizing, and the model radius of 10 nm has exceeded it. Aside from having an enormous turn-on voltage, the entire device is contained within a region of total depletion. Application of a bias will not change this; indeed, as the voltage increases, the semiconductor material will ultimately break down! The significance of the pedestal width is it effectively decreases capacitance and thereby increases required switching energy. The net effect is that the IV curve (Figure 8) would be shifted to the right and, hence, the device must operate in a higher energy regime. The obvious result is that power dissipation becomes a serious design consideration.

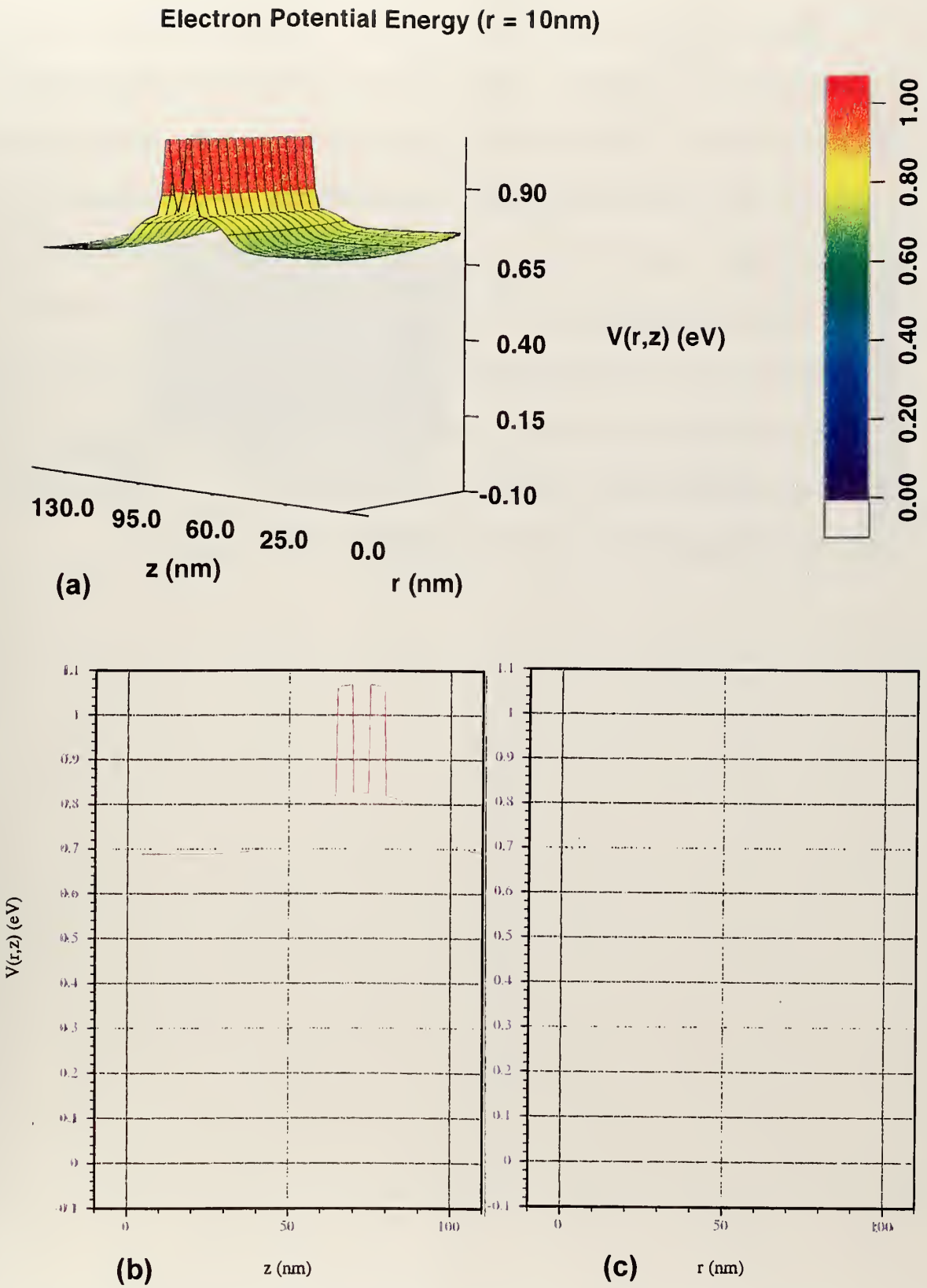

Figure 11 - Plot of a quantum dot with a radius of 10nm. All other variables are the same as Figure 10.

Figure 12, a plot with a radius of 100 nm, shows the presence of many electrons below the Fermi level. This is especially evident in (c), which evinces a conduction radius of about 80 nm - a full 80 percent of the radius! As is illustrated in (b), the device would have an extremely low turn-on voltage, a small fraction of what is required for the device pictured in Figure 10. Unfortunately, the low voltage may be taken to an extreme as is possibly what has happened in this instance. The increased device diameter works toward reducing the separation of states in the quantum well due to lack of lateral confinement. This may have a negative effect on the logic levels as the "on" or "1" voltage level is only marginally greater than the "off" or "0" voltage level.

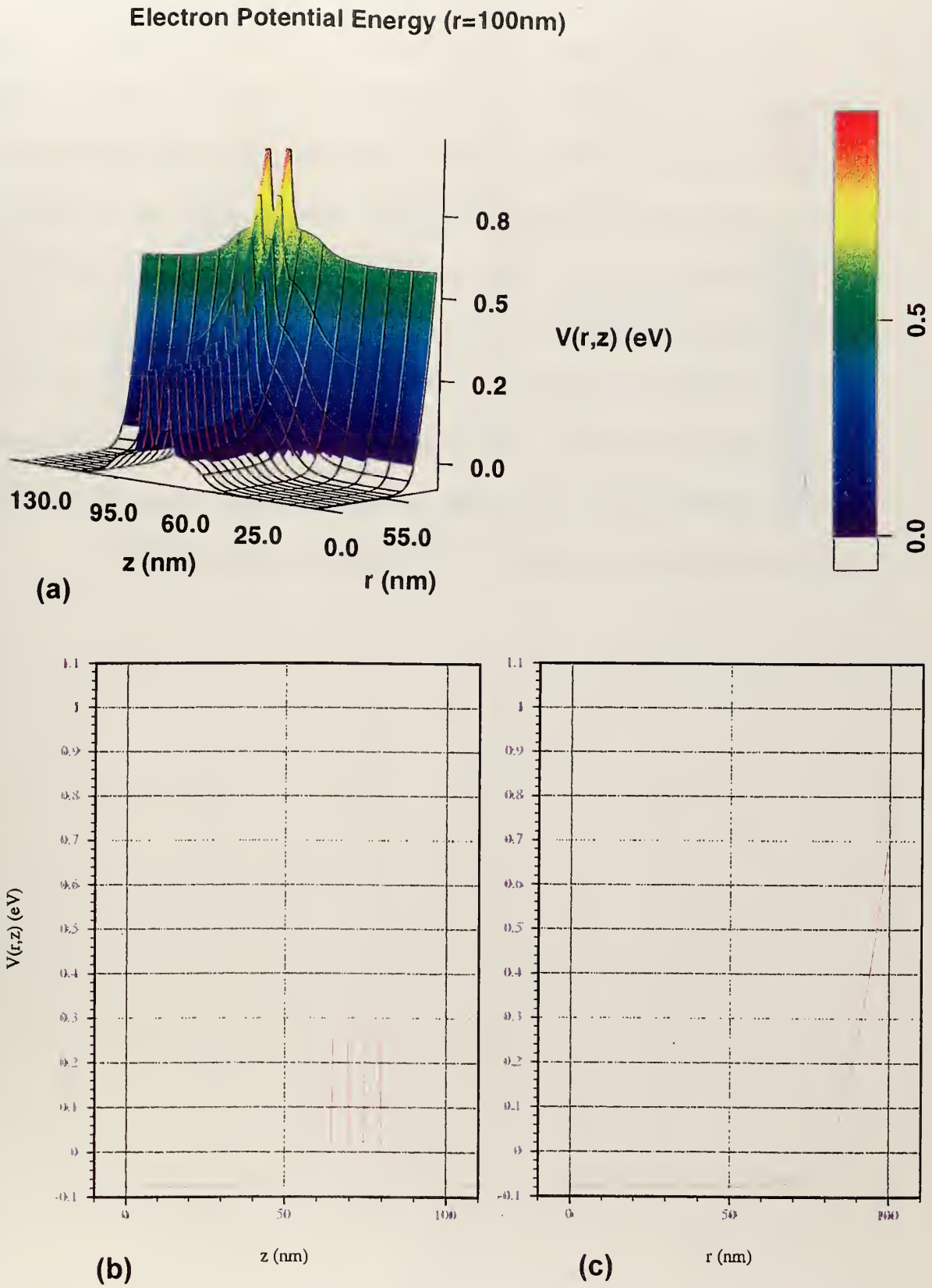

Figure 12 - Plot of a quantum dot with radius 100nm. All other variables are the same as Figure 10.

Figure 13, with a Fermi pinning value of 0.4 eV, is an example of a nearly ideal device. The pedestal in (b) is lower and thinner than that shown in Figure 10 making it easier for electrons to flow. A flat-band region extends closer to the surface of the device showing a conduction radius of about 36 nm, again, a much higher value than that of Figure 10. These factors lead to lower depletion of the structure and greater current flow. The problem with this design is that, while device radius is fairly easy to control, Fermi pinning level is not, as it is a material specific parameter. One possible solution would be to deposit metal around the device forming a thin layer. One could apply a voltage to the metal which would, in effect, modulate the Fermi pinning level at the surface.

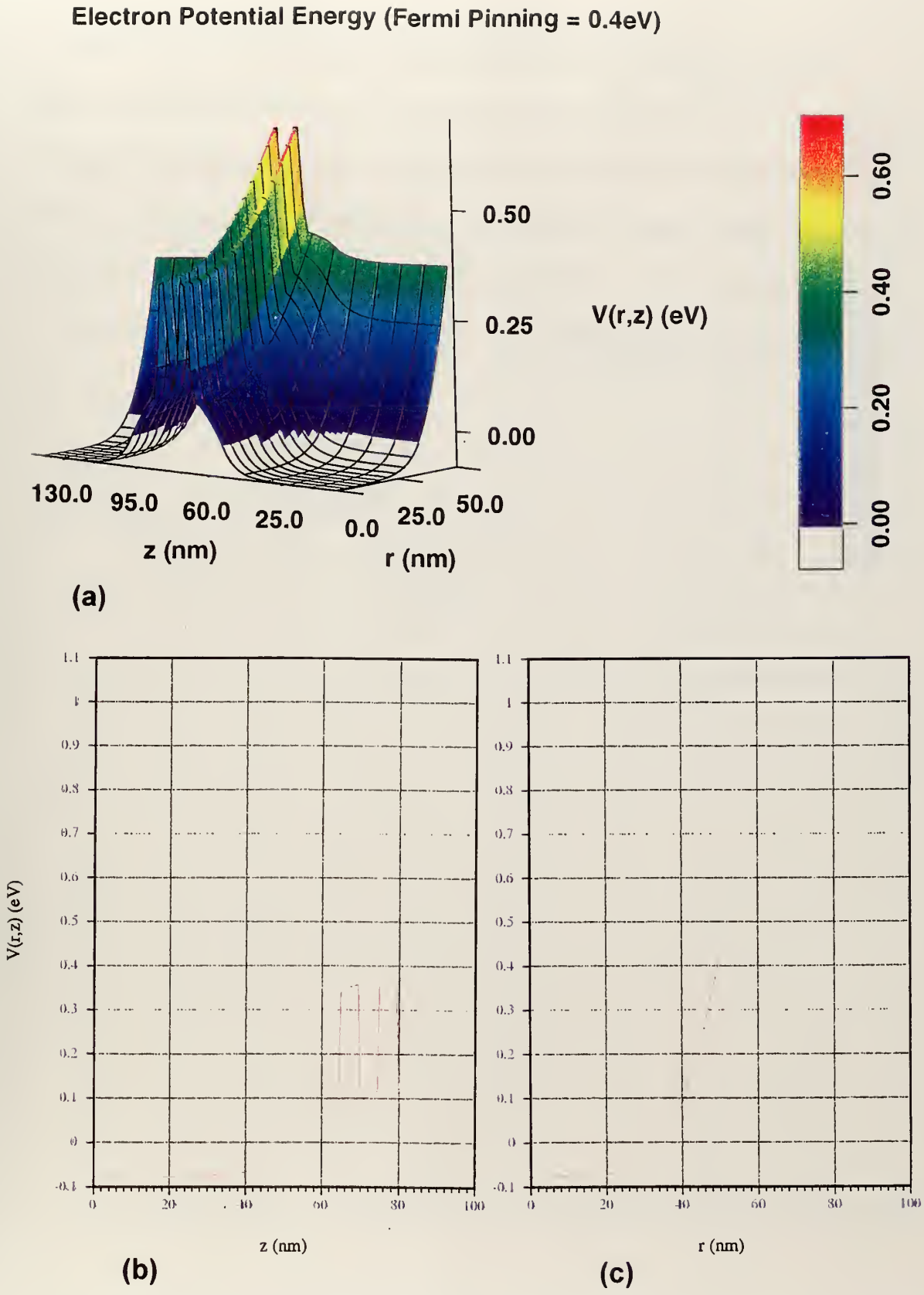

Figure 13 - Plot of a quantum dot with Fermi level pinning value of .4eV. All other variables are the same as Figure 10.

Figure 14 shows a plot with exactly the opposite effect seen in Figure 13 due to the Fermi pinning level being raised to 1.0 eV. The pedestal is very high, which would result in a greater turn-on voltage than that depicted in Figure 10. In fact, the higher pinning level leads to a significantly larger electron depletion region. The conduction radius is about 23 nm, diminishing the number of carriers available for current flow even if the turn-on voltage can be achieved.

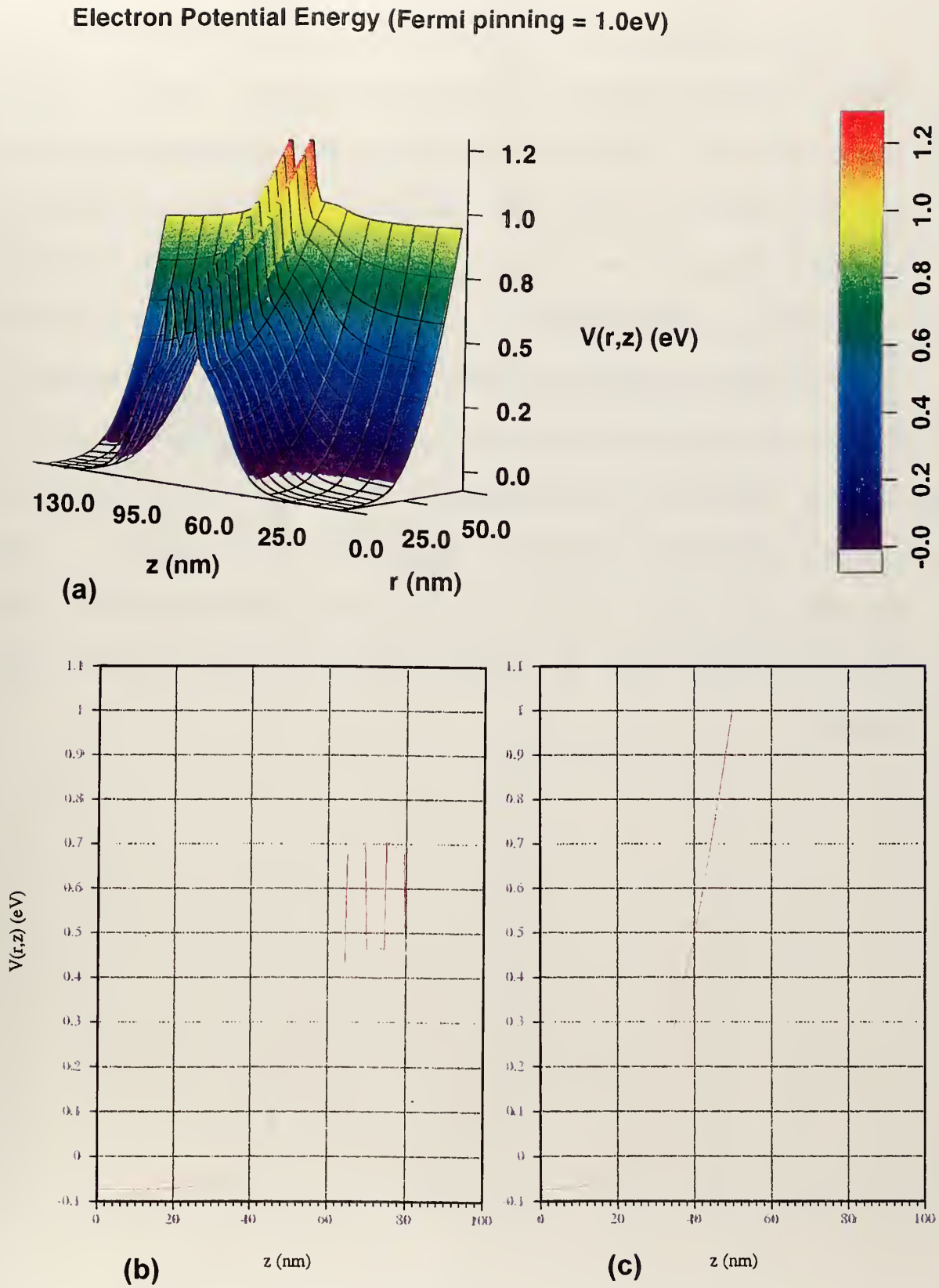

Figure 14 - Plot of a quantum dot with Fermi pinning value of 1.0eV. All other variables are the same as Figure 10.

Figure 15 shows a plot of a device with a spacer width of 1 nm and that would not effectively function as a semiconductor device. Hence, it has no technological utility. The pedestal is down so far, the base of the quantum well extends to beneath the Fermi level. This device would conduct immediately, essentially functioning as a wire, and would lose its valuable nonlinear characteristics. Another problem is there are so many electrons in the quantum well, that electron scattering would broaden the energy width of the resonance, leading to lower peak and higher valley current on the IV curve (as compared to Figure 8). Finally, the turn-on voltage is so low, the device would be unable to operate in a digital logic environment. Notice that (c) is identical to the equivalent plot in Figure 10. This is because spacer width has no effect on the size of the depletion region or conduction radius as will also be evident in the final plot.

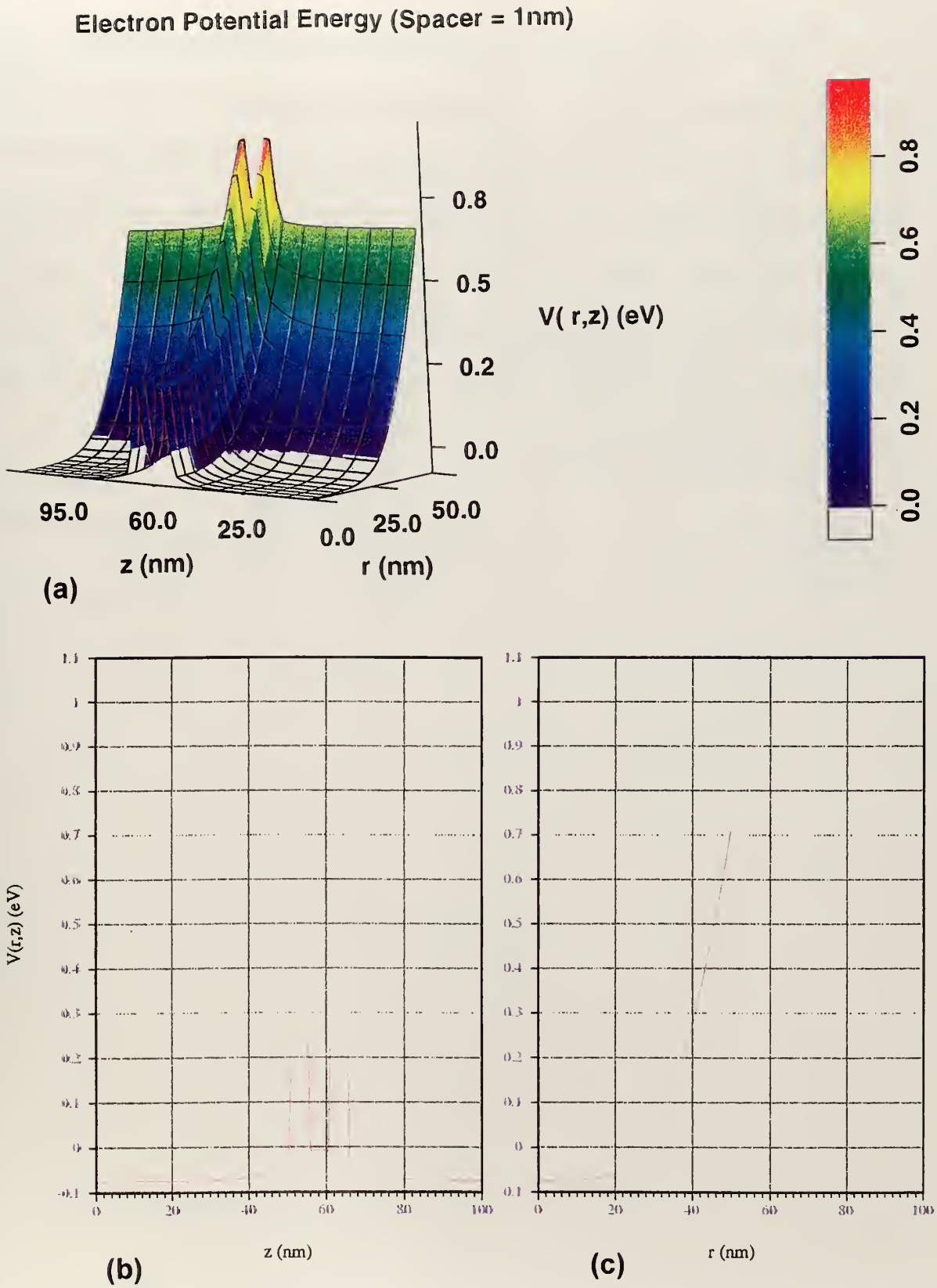

Figure 15 - Plot of a quantum dot with spacer width of 1nm. All other variables are the same as Figure 10.

Figure 16 demonstrates the effect of increasing the spacer width to 30 nm. Not surprisingly, the result is opposite that observed in Figure 15. The turn-on voltage (as shown in the height of the pedestal) to operate this device would be significantly higher than that depicted in Figure 10. The large difference shows that spacer width is a significant design parameter. Also, note the increased width of the pedestal, decreasing the capacitance and thereby increasing required switching energy. Once again, (c) is identical to the corresponding plot in Figure 10.

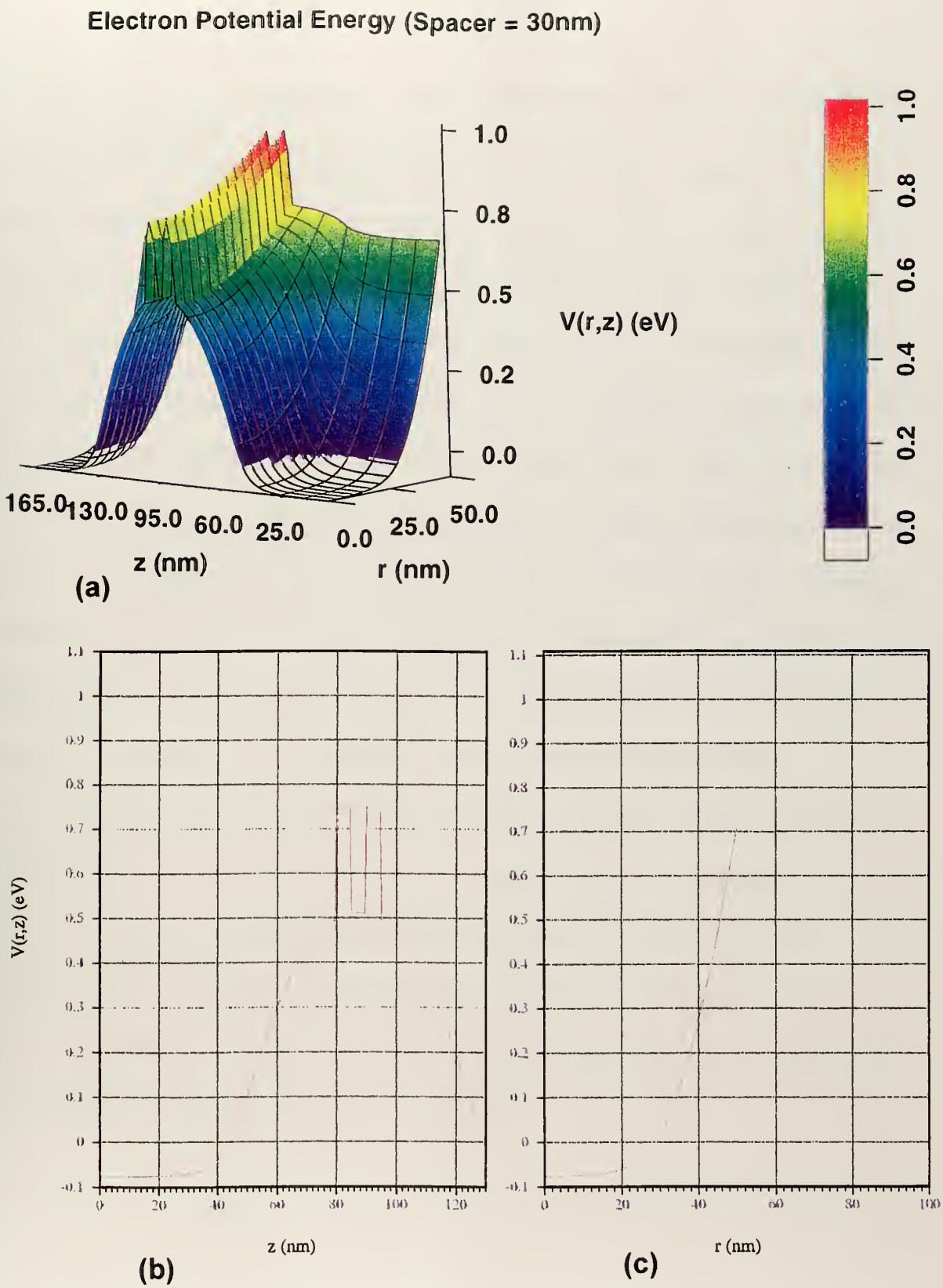

Figure 16 - Plot of a quantum dot with spacer width of 30nm. All other variables are the same as Figure 10.

VII. DISCUSSION

Chapter VI showed that Fermi pinning value, spacer width and device radius are all important design considerations. While Fermi level pinning is the most sensitive of the three, it is difficult to vary the Fermi pinning level in the fabrication process, pending development of a means to apply a metal coating. On the other hand, device radius is fairly easy to alter. One must bear in mind, however, total depletion within the device occurs if the radius is made too small. Increasing the radius beyond the 50 nanometer regime begins to introduce trade-offs, however, and future technology may enable identification of an appropriate device radius. Altering the spacer width is also relatively straightforward, though neither increasing or decreasing the width to a significant degree appears to be of value. Quite possibly, the optimal spacer width will be around 15 nm, regardless of any technical breakthroughs.

The results presented herein underscore the great utility of theoretical modeling. Device modeling incorporating quantum effects is especially superior to the "trial-and-error" approach when designing at the nanoscale level. The model outputs enable one to determine the most sensitive design parameters as well as the effects of varying input data. Continued work in this area might focus on modifying QDOT to incoporate a finite bias.

LIST OF REFERENCES

1. Greiner W., 1995, *Relativistic quantum mechanics wave equations* (Berlin: Springer-Verlag).

2. Luscombe J.H., 1993, "Current Issues in Nanoelectronic Modeling" *Nanotechnology* **4**, 1-20.

3. Ferry D.K. and Grubin H.L., 1995, *Solid State Physics, Advances in Research and Applications* **49**, ed. Ehrenreigh H. and Turnbull D., 283-448.

4. Reed M.A., et.al., 1989, "Quantum Dot Resonant Tunneling Spectroscopy" *Festkörperprobleme* **29**, 267-282.

5. Bate R.T. ed., 1989, *Texas Instruments Technical Journal* **6**, No 4.

6. Frensley W.R., 1994, *Heterostructures and Quantum Devices,* ed. Einspruch N.G. and Frensley W.R. (New York: Academic Press), 1-24.

7. Yu E.T., McCaldin J.O. and McGill T.C., 1992, *Solid State Physics, Advances in Research and Applications* **46**, ed. Ehrenreigh H. and Turnbull D., 2-146.

8. Matyi R.J., 1994, *Heterostructures and Quantum Devices,* ed. Einspruch N.G. and Frensley W.R. (New York: Academic Press), 25-61.

9. Randall J.N., Luscombe J.H. and Bate R.T., 1994, *Heterostructures and Quantum Devices,* ed. Einspruch N.G. and Frensley W.R. (New York: Academic Press), 419-445.

10. Mizuta H. et.al., 1995, *The Physics and Applications of Resonant Tunneling Diodes* (Cambridge: Cambridge University Press).

11. Turton R., 1996, *The Quantum Dot* (New York: Oxford University Press).

12. Seabaugh A.C., Luscombe J.H. and Randall J.N., 1990, "Resonant Tunneling Transistor Logic" A paper delivered at the Government Microcircuit Applications Conference.

13. Luscombe J.H., Bouchard A.M. and Luban M., 1992, "Electron Confinement in Quantum Nanostructures: Self-Consistent Poisson Schrödinger Theory" *Physical Review* **B 46**, 10262-10268.

14. Luscombe J.H. and Luban M., 1990, "Lateral Confinement in Quantum Nanostructures: Self-Consistent Screening Potentials" *Applied Physics Letters* **57** (1), 61-63.

15. Luscombe J.H. and Frensley W.R., 1990, "Models for Nanoelectronic Devices" *Nanotechnology* **1**, 131-140.

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